A HIGH VOLTAGE ESD PROTECTION CIRCUIT WITH LOW VOLTAGE TRANSISTORS

ABSTRACT

[0030] An ESD protection circuit includes a stacked NMOS transistor pair coupled between a pad and a negative voltage supply, with a first transistor's drain connected to the pad and a second transistor's source connected to the negative power supply. A first voltage divider provides reduced voltage from a high voltage positive power supply to a gate of the first transistor, a first diode string coupled between the gates of the first and second transistors, a second diode string with its anode coupled to the pad, an inverter with a source of its PMOS transistor coupled to a cathode of the second diode string and with its NMOS transistor coupled to the negative power supply, an output node of the inverter coupled to a gate of the second transistor, and a RC circuit coupled to an input node of the inverter, for dissipation of ESD current.